

# SAMRAT ASHOK TECHNOLOGICAL INSTITUTE (Engineering College), VIDISHA M.P.

(An Autonomous Institute Affiliated to RGPV Bhopal)

Department of Electronics Engineering

## Syllabus applicable to July 2022 admitted and later batches

Name of the course:			B. Tech in Electronics & Communication Engineering										
Semes	B. Tech 1 <sup>st</sup> Year 2 <sup>na</sup> Semester												
Subject Category				Engineering Science Course (ESC)									
Subject	Subject Name: Digital Electronics												
Maximum Marks Allotted								Contact Hours					
	Theory Practical Total								Juis	Total			
End Sem	Mid- Sem	Assignment	Quiz	End Sem	Lab- Work	Marks	L	Т	Ρ	Credits			
60	20	10	10	30	10	10	150	3	0	2	4		
Prerequ	uisites:												
Applied	Physics, E	Basic Electronic	cs										
Course	Objective	e:											
The obj	ective of t	his course is t	o provid	e the fu	undamer	ntal con	cepts asso	ciated	l with t	he dig	ital logic		
and circ	uit design.	l o familiarize	student	s with th	he differe	ent num	ber system	is, log	ic gates	s, mini	mization		
of logic	The court	ia combination	iai and i	sequen design	and ana	lits utiliz	ea in the digital circ	uite ar	nt aigit nd sveta	al circ	uits and		
Course				uesign		iyze the		unto ai	iu sysi	51113.			
	mpletion	of this course	the stud	ent will	he able t	·O.							
•		vert different n	umbor s	vetome	and coc	 	l in diaital d	rircuite	and ex	vetom	-		
•	CO2: Sim	nlify and analy	ze the c	linital lo		its usin	n Boolean	algehi	and s	other i	s. manning		
	technique	S.	20 110 0	ingital lo	gie en ee	nto donny	g Dooloun	aigobi	a ana		napping		
•	CO3: Ána	lyze and desig	n differe	ent com	bination	al and s	equential	logic c	rcuits	using	different		
	mapping t	echniques and	l mather	natical	tools.			-		-			
•	CO4: Con	npare different	types c	of logic t	families	in the d	omain of p	perform	nance,	efficie	ency and		
	economy.												
									· · ·				
UNIIS			De	escripti	ons				Hr	S.	CO's		
	Introduction to Digital Electronics: Review of number system and										001		
I	conversions; Binary Arithmetic, Signed and Unsigned representation,									10	001		
	correction codes - parity check codes and Hamming code.												
	Boolear	Algebra and	Switc	hina Fi	unctions	<b>s -</b> Stuc	ly of basic	loaic					
	gates, I	Basic postulat	tes and	l funda	mental	theorem	ns of Bo	olean			000		
11	algebra; Standard representation of logic functions - SOP and POS									8 00	002		
	forms; Simplification of switching functions - K-map and Quine-												
	McClusk	ey tabular met	hods.										
	Combinational Logic Modules and their applications: Adders,												
111	Subtract	ors, Code Co	nverters	s, parity	/ genera	ators ar	nd compar	ators,	ç	)	CO3		
	Encoders & Decoders, BCD to seven-segment decoder, Multiplexers												
	Sequent	tial Circuite a	nd Sve	tems: 0	set-Res	at latche	s and flin	flons					
	D-flinflor	R-S flin-flor	) J-K F	-lip-flon	Maste	r slave	Flip flon	edue					
	trigaerec	flip-flop. T f	lip-flops	, Shift	registers	s, class	ification of	f shift		<u> </u>	000		
IV	registers	, Counters,	class	sificatio	n: asy	nchron	ous cou	nters,	1	U	CO3		
	synchror	nous counters,	counter	s desig	n using	flip flops	, Introduct	ion to					
	finite sta	te machines.											
	Logic	families:	C spe	cificatio	on terr	ninology	, Opera	tional			CO4		
V	characte	eristics of BJT	in satu	ation a	ind cut-o	off regio	ns, Opera	tional	0	8			
	cnaracte	eristics of MOS	or⊢las	s switch	i; introd	uction to	o amerent	logic	ogic				

families; TTL, CMOS, ECL, IIL etc., and CMOS gates, comparison of various logic families.	Structure and operations of TTL performance characteristics of						
Guest Lectures (if any)	May be arranged as required						
Total Hours	45						
Suggestive list of experiments:							
1. Study of different digital IC's in term of etc.) Testing of IC's by using IC tester	of their technical specification. (Pin . (CO4)	diagram ap	plication				
2. Study of different digital logic gates an	d verifications of their truth table. (C	;O2)					
<ol><li>To design the basic logic gates using us</li></ol>	iniversal gates and verify their truth	table. (CO2	<u>2)</u>				
4. To design 4-bit two input adder using 2	7483 IC and verify truth table. (CO3	)					
<ol><li>To convert the Binary code to Gray co</li></ol>	de using 7486 IC. (CO1, CO3)						
6. To study and verify the De Morgan's T	heorem. (CO2)						
7. To design the half adder using Univers	al gate. (CO3)						
8. To Design the full adder using Univers	al gate. (CO3)						
9. Verification of state tables of RS, and 10. Verification of state tables of T and D f	IK filp-flops using NAND & NOR ga	(CO3)					
Toxt Book	ip-nops using MAND & NON gates.	(003)					
M Mano "Digital Logic and Computer	Design" Dearson Education						
T I Floyd "Digital Fundamentals" Pe	parson Education						
<ul> <li>A. Anand Kumar, "Fundamentals of Di</li> </ul>	gital Circuits", PHI.						
Reference Books-							
R.J. Tocci, "Digital Systems Principles	&: Applications".						
W.H. Gothman, "Digital Electronics" (F	PHI).						
List and Links of e-learning resources:							
1. https://nptel.ac.in/courses/108/105/	108105132/						
2. https://de-iitr.vlabs.ac.in/							
Modes of Evaluation and Rubric							
The evaluation modes consist of performance in Two mid-semester Tests, Quiz/ Assignments, lab							
work, end-semester examinations, and end-se	mester practical examinations.						
Recommendation by Board of studies on 15.06.2022							
Approval by Academic council on							
Compiled and designed by							



SAMRAT ASHOK TECHNOLOGICAL INSTITUTE											
ETA)		(Engineering College), VIDISHA M.P.									
and the	e.	(An Autonomous Institute Affiliated to RGPV Bhopal)									
Syllabus applicable to July 2022 admitted and later batches											
Semester/Year Program B.Tech.											
Subject	Subject Subject						_				
Category	ategory ESC Code: ECA102 Name: Problem Solving using							ng Da	Jata Structures		
		Maxin	num Ma	rks Allot	ted			Cont	act Ho	oure	
	Theo	ry Accian		Practi			Total Marka	Cont		Juis	Total
End Sem	Sem	ment	Quiz	Sem	Work	Quiz	TOLAT WALKS	L	Т	Ρ	Ciedits
60	20	10	10	30	10	10	150	3	0	2	4
Prerequisite	es:										
Logical thin	king and	Compute	r Funda	mentals	;						
Course Obj	ective:										
Introduce t	he funda	amentals	of data	structu	res and	how	these concep	ts are	usefu	ul in	problem
solving.											-
Course Out	comes:										
CO-1Unde	rstand-	Problem s	solvina	usina a	of data	structu	re and variou	is sea	rchind		sorting
methods	otunia		Johnig	doing c	, uulu	onaota				,	i corting
		different c	onconte	of data	etructu	ree to s	olve different	compu	tina n	roble	me
					rn of y			compu	ung p Lund	oroto	nd their
	iyse- Ai	laiyze lite	acces	s palle		anous	uala siluciu		i unu	ersia	
		L	0		¢						
CO-4 Eval	Jate-Eva	iluate and	Compa	are the p	pertorm	ance of	r different data	a struci	ures	on re	al world
problems.											
CO-5 Discu	<b>iss-</b> Gra	ph and Tre	ee struc	ture wit	h their c	peratio	ns and applica	ability			
UNITS Descriptions								H	lrs.	CO's	
	Problem solving concepts: top-down, bottom-up design, Concept of										
	datatyp	e, variab	le, co	nstant	and p	ointers	. Dynamic	memo	ry		
	allocatio	on.									
	Algorithm: Definition and complexity Analysis										
	Introduction to data structure: Linear Nonlinear Primitive and								bd		
	Nonnrin	nitive				.,				80	
	Arraye	Conconte	of /	\rrave	Singlo	dimo	neional arra	v tva/			
	dimonoi	ional arr		nnays,	totion	and	Addroop Col	y, two			
	Onereti								~		
	Operation	ons on an	ays witt	1 algorit	nms (ua	aversing	g, searching, i	nserun	g,		
	deleting	)) and ana	iysis.								
	List-Sir	ngly linked	l lists:	Repres	entation	in me	emory, Opera	tions c	n		
	singly I	linked list	with a	lgorithm	ns (trav	ersing,	searching, i	nsertio	n,   (	06	
	deletion	n)Doubly li	linked list-Operations with algorithms and analysis.					-			
	Circular	linked	lists-Op	peration	s with	algor	ithms and a	analysi	s.		



	Representation & manipulations of polynomials/sets using linked lists.						
	Stack- Introduction to Stack and its operations, Implementation of						
	stack using array and linked list with comparison. Application of						
	stacks (Polish Notations, converting infix to postfix notation,						
III	evaluating postfix notation, Parenthesis balancing, Recursion).	09					
	Queue- Introduction to Queue and its operations. Implementation of						
	queue using array and linked list. De-queue, circular queue, priority						
	queue. Applications of queue.						
	<b>Tree-</b> Definition and terminology, concept of binary tree and						
	representation, Traversing binary tree(pre order, post order, in order)						
	Operation with algorithm -insertion and deletion. Binary Search Trees						
IV	and Concept of balance tree (AVL).	09					
	Graph- Definition and terminology, Types of graphs, Representation						
	of graph. Traversing of graph- Breadth First Traversing and Depth						
	First Traversing.						
	Searching- Search methods- Linear search, Binary search and						
	Hashing (collision, chaining and probing) with their algorithms and						
V	analysis.	08					
	Sorting-Sorting Methods-Bubble sort, Selection sort, Insertion sort,	rt,   00					
	Quick sort, Merge sort, Radix sort, Shell sort with their algorithms and						
	analysis.						
Guest Lect	ures (if any)						
Total Hour	'S	40					
List of Exp	periments						
1. VVr	nemic memory ellegation	the co	ncepts of				
	namic memory allocation.						
2. VVr		ons:					
	I. Traverse an array.	~~					
	ii. Find minimum item, maximum item, and average of an array item	ns.					
'	in. Insert a new item at beginning, end and middle position within an	i allay.					
3 Wr	ite a program to implement singly linked list with following operations						
i 0. 10	Insert a new item at beginning, end and middle position within a s	sinale li	nked list				
	Delete an item from single linked list.						
ii	i. Traverse a single linked list.						
4. Mo	Modify the singly linked list program to make it for doubly linked list.						
5. Wr	Write a program to implement Stack with its operations (Push, Pop, Peek, IsEmptv) using:						
1	the a program to implement otack with its operations (1 dsn, 1 op, 1 eek, 1		-				
i.	Using array						
i. ii.	Using array Using linked list						
i. ii. 6. Wr	Using array Using linked list ite a program to evaluate postfix notation using stack.						
i. ii. 6. Wr 7. Wr	Using array Using linked list ite a program to evaluate postfix notation using stack. ite program to implement queue with its operations (enqueue, dequeue)	using:					



- ii. Using linked list
- 8. Modify the queue program to implement circular queue with its operations.
- 9. Write a program to implement binary search tree with insert and delete operations.
- 10. Write a program to implement depth first traverse and breadth first traverse on a graph.
- 11. Write program to implement linear search and binary search on a given array.

12. Write a program to sort a given list of 10000 random integers and compare their execution time using:

- i. Bubble sort
- ii. Insertion sort
- iii. Merge sort
- iv. Quick sort
- v. Radix sort

Reference Books-

- Data Structure- Schaum's Series- McGraw Hill Publication
- Data Structure- Horwitz and Sartaj Sahni
- Data Structure through C, Yashwant Kanekar, BPB Publication.

Modes of Evaluation and Rubric

The evaluation modes consist of performance in Two mid-semester Tests, Quiz/ Assignments, term work, end-semester examinations, and end-semester practical examinations.

List/Links of e-learning resource

Recommendation by Board of studies on	June-2022
Approval by Academic council on	June-2022
Compiled and designed by	
Subject handled by department	





# SAMRAT ASHOK TECHNOLOGICAL INSTITUTE (Engineering College), VIDISHA M.P.

(An Autonomous Institute Affiliated to RGPV Bhopal)

#### Department of Electronics Engineering

## Syllabus applicable to July 2022 admitted and later batches

Name of the course:			B. Tech in Electronics & Communication Engineering								
Semester and Year of study				B. Tech 1 <sup>st</sup> Year 2 <sup>nd</sup> Semester							
Subject Category				Engineering Science Course (ESC)							
Subject Code: FCI 110				Subject Name: Electronics Workshop							
Maximum Marks Allotted											
		Theory			Practical			Hours			Total
End	Mid-			Fnd	Lab-		Total	-		_	Credits
Sem	Sem	Assignment	Quiz	Sem	Work	Quiz	Marks	L	T	Р	
-	<u>30</u> 10 10 <b>50</b> 1 0 2 <b>2</b>										
			1	1				1		1	
Prereq	uisites:										
Applied	d Physic	cs, Basic Elect	ronics								
Course	Object	ive:									
The air	n of the	course conten	t is to de	evelop di	fferent typ	oes of sl	kills leadin	g to	the a	chiev	ement of
the foll	owing c	ompetency:									
(i)	Te	est various elec	trical an	d electro	onics com	ponents	, and mea	asure	e circu	ıit paı	ameters.
(ii)	Ab	ole to identify va	arious R	esistors,	capacito	rs, induc	ctors and t	rans	forme	ers et	c Use of
	ins	struments such	i as anal	og & dig	ital multin	neter, C	RO and F	unct	ion ge	enera	tor, etc.
(iii)	Int	terpret data sh	eet of va	arious el	ectronics	compor	ients, diffe	erent	ICs a	and t	neir
(5.4)	schematic/ pin diagram.										
		nos:	aiu, PCE	uesign	Soliwale			elect	TOTICS	s com	ponents.
Course Outcomes:											
Arter completion of the course the students will be able to:											
1.	<ol> <li>iterative electronics components schematic symbols and interpret its parameters using data sheets. Perform their testing using lab instruments.</li> </ol>										
2	udia sheets. Periorni their testing using iab instruments.										
3.	Describe PCB design technique and assemble the electronic circuits										
4.	Locate	the fault and t	roubles	noot the	circuit boa	ard.			-		
5.	Desigr	n and complete	a mini-	project.							
Sugge	stive list	of experiment	s:								
1.	Identifi	ication, Stud	dy an	d Tes	sting o	f var	ious el	ectro	onic	cor	nponents:
	(a) Re	sistances-Vari	ous type	es, Color	coding (t	o) Capa	citors-Vari	ious	types	, Col	or coding,
	(c) Inc	ductors (d) Did	odes (e)	Transis	stors (f) S	SCRs (g	g) ICs (h)	Ph	oto d	iode	(i) Photo
	transis	stor (j) LED (k)	LDR (I)	Potentio	meters (m	ו) PID d	iagram, et	tc. (C	CO1)		
2.	Study	of symbols for	various	Electrica	I & Electr	onic Co	mponents	, De	vices,	etc.	(CO1)
3.	Assem	bling and Test	ting of V	arious C	ircuits su	ch as di	ode clippi	ng a	nd cla	ampir	g circuits
4	on Bre	ad board / Circ	cuit Simi	ulators. (	CO2)	ala ha-	tainly (Of	าวง			
4.	(a) Sti	uay of soldering	g compo	onents, s	olders, to	ois, nea	t sink. (CC	J3)			
5	(D) 50	sign and fabric	-soluenn	PCB for	;e. a given ci	ircuit (C	·O3)				
5.	<ul> <li>a) Design and tabrication of PCB for a given circuit. (CO3)</li> <li>(b) Assemble the given circuit on PCP and test it. (CO2)</li> </ul>										
6	Study	of electronic to	est and	measuri		ment M	) Iultimeter	05	rilloso	one	Function
0.	Gener	ator and Regul	lated Po	wer Sun	plv. (CO1	)	anneter,	03	511030	ope,	
7.	Study	PCB designing	g softwa	re and a	enerate th	ne routin	g layout.	CO2	2, CO	3)	
8.	Perfor	m the troubles	hooting	of circuit	and unde	erstand s	safety asp	ects	. (CO	4)	
9.	Study	of component	data she	eet and it	ts interpre	etation (0	CO1)	_	<b>、</b> -	,	
10.	Desig	n and assembl	y of a m	ini projec	ct. (CO5)	,					
				-							
Text Bo	ooks-										
1.	1. Troubleshooting Electronic Equipment by R. S. Khandpur, MHE, India							3			

Testing of Electronic Components, Sarkar and Fernandes, Shroff Publishers 2. 3. Basic Electronic Components, V.K. Barbudhe, Notion Press Reference Books-1. Beginner's Guide to consumer electronics repair, K. Douglas, iUniverse publishers 2. A guide to Electronic Maintenance and Repair, A. M. Yousufu and Y. Ali S., Author House Publishers. 3. How to Diagnose and Fix Everything Electronic, M. J Geier, MGH List and Links of e-learning resources: 1. https://www.circuitlab.com/ 2. https://www.partsim.com/simulator 3. https://www.tinkercad.com/learn/circuits 4. https://circuitmaker.com/ 5. https://www.datasheets.com/ Modes of Evaluation and Rubric The evaluation modes consist of performance in lab work and end-semester practical examinations. Recommendation by Board of studies on 15.06.2022 Approval by Academic council on Compiled and designed by

